In re Patent Application of:
**MARIAUD ET AL.**
Serial No. **09/989,317**
Filing Date: **NOVEMBER 20, 2001**

## REMARKS

The Examiner is again thanked for the thorough examination of the present application. Independent Claims 5, 11, 17, 20 and 22 have been amended to more clearly define the subject matter thereof over the prior art. Support for the amendments may be found beginning on page 4, lines 9-16 of the originally filed specification, for example. No new matter is being added.

In view of the amendments and the supporting arguments presented in detail below, it is submitted that all of the claims are patentable.

## I. The Claimed Invention

The present invention is directed to a computer system. As recited in amended independent Claim 5, for example, the computer system includes a master apparatus and a slave apparatus for communicating therewith via a universal serial bus (USB) protocol. The slave apparatus includes a sending/receiving circuit for sending and receiving binary information to and from the master apparatus and supplying status signals based thereon. Moreover, a plurality of state latches and control circuitry cooperating therewith receive the status signals from the sending/receiving circuit and supply state signals of the sending/receiving circuit based thereon. The slave apparatus further includes a microprocessor for processing applications of the slave apparatus and also for processing the binary information received by the sending/receiving circuit when an

interruption signal is supplied. Furthermore, an interruption state latch and a control circuit cooperating therewith supply an interruption signal to the microprocessor once the start of a new message has been acknowledged and recorded by the sending/receiving circuit. The sending/receiving circuit also acknowledges the start of a following message while the interrupt signal is supplied.

Independent Claim 11 is directed to a similar computer system, independent Claim 17 is directed to a similar slave apparatus, and independent Claims 20 and 22 are directed to related methods. Each of these claims has been amended similarly to Claim 5 to recite acknowledging the start of a following message while the interrupt signal is supplied.

## II. The Claims Are Patentable

The Examiner rejected independent Claims 5, 11, 17, 20 and 22 over the prior art discussed in the background of the present application (the "admitted prior art"). The admitted prior art describes a typical master-slave computer system arrangement, such as the one illustrated in FIG. 1 of the present application. Beginning on page 2, line 29, it is noted that during different transfer stages between the master apparatus and the slave apparatus, there are provisions which allow the master apparatus to repeat its part of the message IN and OUT while the microcontroller (i.e., microprocessor) of the slave apparatus is unavailable. If the phase that follows is a start phase and its microcontroller is unavailable, the slave apparatus returns no

signal (no NAK, nor STALL, nor ACK signal), which is interpreted by the master apparatus as a transmission error. In such case the master apparatus resends the message.

Such an operation only appears if the time period during which the slave microcontroller is unavailable exceeds a time interval separating two consecutive messages. However, in high-speed data transfers, these time intervals between two messages are increasingly short. Yet, the microcontroller of the slave apparatus has to perform more and more tasks, while the time periods during which it is unavailable are longer and longer.

At the end of the transfer stages, an interruption of the microcontroller to process the part of the transmitted message may be requested. To this end, a flag CTR is set to the logic 1 state to indicate that an interruption is requested (see FIG. 3(d) of the present application). After a certain time (which depends on the application), the interruption requested by the USB bus is processed. At the end of the interruption, the program executed by the microcontroller returns the flag CTR to the logic 0 state, thus authorizing the transfer of the following part of the message. A software state machine then processes the information concerning the event of the USB message extracted by the interruption routine.

As a result of the above operations, no transfer over the USB bus is authorized when the flag is in the logic 1 state. There is, therefore, a dependency between the time for processing an interruption and the time delay in accepting the following transfer, the time for processing the interruption being linked

to the microcontroller's operating frequency. Further, the time delay between each transaction depends on the master apparatus in that if that time delay is shorter than the minimum time for processing an interruption by the microcontroller, the following transfer cannot be authorized. This can result in the failure of the transaction.

The above-noted independent claims have been amended to recite processing a new message when an interrupt signal is supplied, and acknowledging the start of a following message while the interrupt signal is supplied. The claimed invention thereby allows, at the end of a message, an acceptance of the start of a following message while the microcontroller is unavailable, in stark contrast to the admitted prior art, as discussed above. See, e.g., page 4, lines 9-16 of the originally filed specification.

As such, it is respectfully submitted that the admitted prior art fails to teach all of the recitations of independent Claims 5, 11, 17, 20 and 22 as amended. Since the remaining prior art of record fails to teach or fairly suggest the deficiencies of the admitted prior art, it is respectfully submitted that these claims are patentable. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

## CONCLUSIONS

In view of the foregoing, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor

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informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

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**CERTIFICATE OF FACSIMILE TRANSMISSION**

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the Commissioner for Patents this 1 day of March, 2006.